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(54) Title: USE OF METALLIC TREATMENT ON COPPER FOIL TO PRODUCE FINE LINES AND REPLACE OXIDE PROCESS IN PRINTED CIRCUIT BOARD PRODUCTION

(57) Abstract: The invention relates to the manufacture of printed circuit boards having enhanced etch uniformity and resolution. The process eliminates the need for a black oxide treatment to improve adhesion and improves the ability to optically inspect the printed circuit boards. The process is performed by conducting steps (a) and (b) in either order: a) depositing a first surface of an electrically conductive layer onto a substrate, which electrically conductive layer has a roughened second surface opposite to the first surface; b) depositing a thin metal layer onto the roughened second surface of the electrically conductive layer, which metal layer comprises a material having a different etch resistance property than that of the electrically conductive layer. Thereafter one deposits a photoresist onto the metal layer; imagewise exposes and develops the photoresist, thereby revealing underlying portions of the metal layer. The one removes the revealed underlying portions of the metal layer, thereby revealing underlying portions of the conductive layer and removes the revealed underlying portions of the conductive layer, to thereby produce a printed circuit layer.

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USE OF METALLIC TREATMENT ON COPPER FOIL TO PRODUCE FINE LINES AND REPLACE OXIDE PROCESS IN PRINTED CIRCUIT BOARD PRODUCTION

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The present invention relates to the manufacture of printed circuit boards having enhanced etch uniformity and resolution. The process of this invention eliminates the need for a black oxide treatment to improve adhesion and improves the ability to optically inspect the printed circuit boards.

DESCRIPTION OF THE RELATED ART

Printed circuit boards have wide application in the field of electronics. They are useful for large scale applications, such as in missiles and industrial control equipment, as well as in small scale devices, such as telephones, radios and personal computers. In particular, when utilizing printed circuits it is important that a high degree of accuracy and resolution is attained for very small line and space widths (on the order of one hundred microns or less) to ensure good performance of the circuit.

The ability to produce accurate features having very small dimensions, on the order of one hundred microns or less, is extremely important in the production of small and large scale equipment. The precision of the etching process becomes more important as the circuit patterns become ever smaller. It is well known in the art to use known photolithographic techniques to produce printed circuit boards having small features with high accuracy. In general, an electrically conductive foil is deposited onto a substrate and a photoresist is

then deposited onto the foil. That photoresist is then imagewise exposed and developed, forming a pattern of small lines and spaces that are then etched into the conductive foil.

Conventionally a matte side of a foil is laminated onto the substrate, mainly because the matte side of the foil is rougher and has better adhesion to the substrate than the shiny side of the foil. However, it has been found that by laminating the foil with the shiny side down against the substrate that much more accurate etching could be achieved because the copper grains are elongated and oriented vertically near the matte side and less side or horizontal etching occurs. In addition, there is less of a need to over etch to remove the tooth structure and treatment from the substrate, which results in better etch uniformity.

When laminating the shiny side of the foil onto a substrate, it is necessary to roughen the surface to provide sufficient adhesion. One method to accomplish this is to plate nodules to the shiny side of a copper foil. An example of this type of copper product is commercially available from Oak-Mitsui Inc., of Hoosick Falls, N.Y. as MLS. Another method that has been used is to deposit roughening layers, such as nodules, on each side of the foil, forming "double treated" foils. With this process one gets superior resist adhesion, as well as the elimination of the oxide process. This has not been preferred in the industry because the exposed side of the foil may have the roughening layer damaged during handling.

When the matte side is against the laminate another known method of roughening the shiny layer is a process in which a copper foil is pre-roughened by chemical micro etching (using sodium persulfate or sulfuric acid/hydrogen peroxide which are available from MacDermid of Waterbury CT or Shipley

Ronel of Marborough MA) or pumice scrubbing (machines available from I.S of Italy and Isioki of Japan) . The surface is later chemically treated to deposit a layer of black copper oxide (also available from MacDermid and Shipley Ronel), allowing another insulating substrate to be laminated over the circuit. This sequence of chemical treatments is undesirable because it is cumbersome and introduces waste disposal problems with the chemicals used. Therefore, there is a need in the art for a process that does not have the problems of double treating a conductive foil and which does not need a black oxide treatment during the processing of multi-layer circuit boards, that will etch circuit lines and spaces with high resolution and accuracy.

Efforts are continuously being made in the art to improve techniques by which circuit boards are manufactured and thus the accuracy of these features. For example, see U.S. patent 5,240,807 which teaches a photoresist article having a portable, conformable, built-on etch mask useful for enhancing image contrast and reproducing parts having very small dimensions. Portions of a conductive foil underlying the photoresist are selectively etched to form a pattern of circuit lines. Another approach is disclosed in U.S. patent 6,042,711 which provides a metal foil with improved peel strength having a metal layer of a dusty dendritic deposit and a metal flash layer. Additionally, International Publication WO 00/03568 discloses a method of forming circuit lines on a substrate by applying a roughened conductive metal layer using a copper foil carrier.

In yet another approach, U.S. patent 5,679,230 provides a copper foil for use in the manufacture of printed circuit boards. This copper foil can be used to make multilayer circuit boards without requiring the conventional black oxide treatment to improve adhesion.

The present invention provides an approach to solving the problems of the prior art wherein a thin metal layer is deposited onto a conductive layer on a substrate. This metal layer acts as an etch mask during etching of the conductive layer, and improves etch accuracy and resolution. After etching, this thin metal layer remains on the conductive layer obviating the need for an oxide layer.

The metal layers employed in this process are also highly uniform and reflective, making the printed circuits formed thereby more compatible with automatic optical inspection equipment than printed circuits of the prior art. Further, the metal layers used herein have high mechanical strength, and are highly resistant to mechanical damage, such as surface scratches and scuff marks.

SUMMARY OF THE INVENTION

The invention provides a process for producing a printed circuit layer comprising conducting steps (a) and (b) in either order:

a) depositing a first surface of an electrically conductive layer onto a substrate, which electrically conductive layer has a roughened second surface opposite to the first surface;

b) depositing a thin metal layer onto the roughened second surface of the electrically conductive layer, which metal layer comprises a material having a different etch resistance property than that of the electrically conductive layer; and then

c) depositing a photoresist onto the metal layer;

d) imagewise exposing and developing the photoresist, thereby revealing underlying portions of the metal layer;

e) removing the revealed underlying portions of the metal layer, thereby revealing underlying portions of the conductive layer; and

f) removing the revealed underlying portions of the conductive layer, to thereby produce a printed circuit layer.

The invention also provides a printed circuit layer produced by the process of conducting steps a) and b) in either order:

a) depositing a first surface of an electrically conductive layer onto a substrate, which electrically conductive layer has a roughened second surface opposite to the first surface;

b) depositing a thin metal layer onto the roughened second surface of the electrically conductive layer, which metal layer comprises a material having a different etch resistance property than that of the electrically conductive layer; and then

c) depositing a photoresist onto the metal layer;

d) imagewise exposing and developing the photoresist, thereby revealing underlying portions of the metal layer;

e) removing the revealed underlying portions of the metal layer, thereby revealing underlying portions of the conductive layer; and

f) removing the revealed underlying portions of the conductive layer.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The invention broadly provides a process for producing a printed circuit layer and printed circuit board.

The first step in conducting the process of the present invention is to deposit a layer of an electrically conductive material onto a suitable substrate. Typical substrates are those suitable to be processed into a printed circuit or other microelectronic device. Suitable substrates for the present invention non-exclusively include polymers reinforced with materials such as fiberglass, aramid (Kevlar), aramid paper (Thermount), polybenzoxolate paper or

combinations thereof. Of these epoxy with fiberglass reinforcement is the most preferred substrate. Also suitable are semiconductor materials such as gallium arsenide (GaAs), silicon and compositions containing silicon such as crystalline silicon, polysilicon, amorphous silicon, epitaxial silicon, and silicon dioxide (SiO_2) and mixtures thereof. The preferred thickness of the substrate is of from about 10 to about 200 microns, more preferably from about 10 to about 50 microns.

The conductive layer preferably comprises a material such as copper, zinc, brass, chrome, , nickel, aluminum, stainless steel, iron, gold, silver, titanium and combinations and alloys thereof. Most preferably, the conductive layer is a copper foil.

Copper foils are preferably produced by electrodepositing copper from solution onto a rotating metal drum. The side of the foil next to the drum is typically the smooth or shiny side, while the other side has a relatively rough surface, also known as the matte side. This drum is usually made of stainless steel or titanium which acts as a cathode and receives the copper as it is deposited from solution. An anode is generally constructed from a lead alloy. A cell voltage of about 5 to 10 volts is applied between the anode and the cathode to cause the copper to be deposited, while oxygen is evolved at the anode. This copper foil is then removed from the drum, cut to the required size, and laminated onto the substrate. Lamination is preferably conducted in a press at a minimum of about 175°C, for about 30 minutes. Preferably, the press is under a vacuum of at least 28 inches of mercury, and maintained at a pressure of about 150 psi.

Preferably but not necessarily prior to lamination, the conductive foil is preferably, but not necessarily, electrolytically treated on the shiny side to form

a roughening copper deposit, and electrolytically treated on the matte side to deposit micro nodules of a metal or alloy. These nodules are preferably copper or a copper alloy, and do not add roughness to the surface, but do increase adhesion to a substrate. The surface microstructure of the foil is measured by a profilometer, such as a Perthometer model M4P or S5P which is commercially available from Mahr Feinpruef Corporation of Cincinnati, Ohio. Topography measurements of the surface grain structure of peaks and valleys are made according to industry standard IPC-TM-650 Section 2.2.17 of the Institute for Interconnecting and Packaging Circuits of 2115 Sanders Road, Northbrook, Illinois 60062. In the measurement procedure, a measurement length Im over the sample surface is selected. Rz defined as the average maximum peak to valley height of five consecutive sampling lengths within the measurement length Im (where Io is Im/5). Rt is the maximum roughness depth and is the greatest perpendicular distance between the highest peak and the lowest valley within the measurement length Im. Rp is the maximum leveling depth and is the height of the highest peak within the measuring length Im. Ra, or average roughness, is defined as the arithmetic average value of all absolute distances of the roughness profile from the center line within the measuring length Im.

The parameters of importance for this invention are Rz and Ra. The surface treatments carried out produce a surface structure having peaks and valleys, which produce roughness parameters wherein Ra ranges from about 1 to about 10 microns and Rz ranges from about 2 to about 10 microns.

The surface treatments carried out produce a surface structure having peaks and valleys, on the shiny side, which produce roughness parameters wherein Ra ranges from about 1 to about 4 microns, preferably from about 2 to about 4 microns, and most preferably from about 3 to about 4 microns. The Rz value

ranges from about 2 to about 4.5 microns, preferably from about 2.5 to about 4.5 microns, and more preferably from about 3 to about 4.5 microns.

The surface treatments carried out produce a surface structure having peaks and valleys, on the matte side, which produce roughness parameters wherein Ra ranges from about 4 to about 10 microns, preferably from about 4.5 to about 8 microns, and most preferably from about 5 to about 7.5 microns. The Rz value ranges from about 4 to about 10 microns, preferably from about 4 to about 9 microns, and more preferably from about 4 to about 7.5 microns.

Preferably, the shiny side has a copper deposit about 2 to 4.5 μm thick to produce an average roughness (Rz) of 2 μm or greater. The matte side preferably will have a roughness Rz as made of about 4-7.5 μm. The micro nodules of metal or alloy will have a size of about 0.5 μm. Other metals may be deposited as micro nodules if desired, for example, zinc, indium, tin, cobalt, brass, bronze and the like. This process is more thoroughly described in U.S. patent 5,679,230, which is incorporated herein by reference. The shiny surface has a peel strength ranging from about .7 kg/linear cm to about 1.6 kg/linear, preferably from about .9 kg/linear cm to about 1.6 kg/linear. The matte surface has a peel strength ranging from about .9 kg/linear cm to about 2 kg/linear, preferably from about 1.1 kg/linear cm to about 2 kg/linear. Peel strength is measured according to industry standard IPC-TM-650 Section 2.4.8 Revision C.

The conductive layer preferably has a thickness of from about 0.5 to about 200 microns, more preferably from about 9 to about 70 microns. The conductive layer may also be applied using any other well known method of metal deposition such as electroless deposition, coating, sputtering, evaporation or by lamination onto the substrate.

Also preferably but not necessarily prior to lamination, the foil is preferably, but not necessarily, electrolytically treated on either side with, a thin metal layer. This metal layer is preferably electrolytically deposited onto the conductive layer. The metal layer may also be deposited onto the conductive layer (after laminating to the substrate) by coating, sputtering, evaporation or by lamination onto the conductive layer. Preferably the metal layer is a thin film and comprises a material selected such as nickel, tin, palladium platinum, chromium, titanium, molybdenum or alloys thereof. Most preferably the metal layer comprises nickel or tin. The metal layer preferably has a thickness of from about .01 to about 10 microns, more preferably from about .2 to about 3 microns. This metal layer will serve as an etch mask to define a pattern of circuit lines and spaces to be etched into the conductive layer.

Once the metal layer is deposited onto the conductive layer, the next step is to selectively etch away portions of the metal layer, forming an etched pattern in the metal layer. This etched pattern is formed by well known photolithographic techniques using a photoresist composition. First, a photoresist deposited directly onto the thin metal layer. The photoresist composition may be positive working or negative working and is generally commercially available. The resist can be very thin (5 to 20 microns) since it's main function is to only define the thin metal layer and does not need to withstand severe etch conditions. This allows much greater resolution. Suitable positive working photoresists are well known in the art and may comprise an o-quinone diazide radiation sensitizer. The o-quinone diazide sensitizers include the o-quinone-4-or-5-sulfonyl-diazides disclosed in U. S. Patents Nos. 2,797,213; 3,106,465; 3,148,983; 3,130,047; 3,201,329; 3,785,825; and 3,802,885. When o-quinone diazides are used, preferred binding resins include a water insoluble, aqueous alkaline soluble or swellable

binding resin, which is preferably a novolak. Suitable positive photodielectric resins may be obtained commercially, for example, under the trade name of AZ-P4620 from Clariant Corporation of Somerville, New Jersey as well as Shipley I-line photoresist. Negative photoresists are also widely commercially available.

The photoresist is then imagewise exposed to actinic radiation such as light in the visible, ultraviolet or infrared regions of the spectrum through a mask, or scanned by an electron beam, ion or neutron beam or X-ray radiation. Actinic radiation may be in the form of incoherent light or coherent light, for example, light from a laser. The photoresist is then imagewise developed using a suitable solvent, such as an aqueous alkaline solution, thereby revealing underlying portions of the metal layer.

Subsequently, the revealed underlying portions of the metal layer are removed through well known etching techniques while not removing the portions underlying the remaining photoresist. Suitable etchants non-exclusively include acidic solutions, such as cupric chloride (preferable for etching of nickel) or nitric acid (preferable for etching of tin). Also preferred are ferric chloride or sulfuric peroxide (hydrogen peroxide with sulfuric acid). During this step, the portions of the conductive layer underlying the etched off portions of the metal layer are revealed. This patterned metal layer defines an excellent quality etch mask for etching the conductive layer with high accuracy and precision.

Next, the revealed underlying portions of the conductive layer are removed by etching while not removing the portions of the conductive layer underlying the non-removed portions of the metal layer. Suitable etchants for removing the conductive layer non-exclusively include alkaline solutions, such as

ammonium chloride/ammonium hydroxide. This circuit board may then be rinsed and dried. The result is a printed circuit board having excellent resolution and uniformity, and having excellent performance.

In another preferred embodiment wherein the metal layer comprises nickel, a one pass etching process may be conducted. In this embodiment, after the photoresist has been imaged and developed, each of the revealed portions of the metal layer and the underlying electrically conductive layer may be etched in a cupric chloride etcher. For etching of other metal layers, including Tin, the appropriate etchant is unable to properly etch the underlying conductive foil and a second etching step is still required. This single etching step is preferred for etching lines or spaces of greater than about 3 mils. When a single etching step is used, it may also be necessary to increase the dwell time in the etcher by possibly 10 to 25% depending on the etch system. .Higher spray pressures and temperature may accomplish the same results.
After the circuit lines and spaces are etched through the metal layer and the conductive layer, the remaining photoresist can optionally be removed from the metal layer surface either by stripping with a suitable solvent or by ashing by well known ashing techniques. The photoresist may also be removed after etching the metal layer, but prior to etching the conductive foil.

In a preferred ashing process, plasma is generated in a microwave plasma generator located upstream of a stripping chamber and stripping gases pass through this generator so that reactive species produced from the gases in the plasma enter the stripping chamber. Plasma ions are removed such as by filtering from plasma radicals. The term "radical", as used herein is intended to define uncharged particles such as atoms or molecular fragments which are generated by the upstream plasma generator. The plasma generator may comprise any plasma generator known in the art. Plasma generators which are

capable of providing a source of radicals, substantially without ions or electrons, are described, for example, in U.S. patent 5,174,856 and U.S. patent 5,200,031, the disclosures of which are hereby incorporated by reference. While any type of conventionally generated plasma may, in general, be used in the practice of the invention, preferably the plasma used is generated by a microwave plasma generator such as, for example, a Model AURA plasma generator commercially available from the GaSonics of San Jose, Calif. Another upstream plasma generator which is capable of supplying a source of radicals in the substantial absence of electrons and/or ions is commercially available from Applied Materials, Inc. as an Advanced Strip Passivation (ASP) Chamber. Plasma ashers are also commercially available from Mattson Technology of Fremont, California. Ashing may also be performed in an anisotropic method through the use of in situ ashing in an etch chamber such as a TEL DRM 85, available from Tokyo Electron Ltd.

At this point, another insulating substrate may be laminated over the circuit without an additional roughening step and without black oxide treatment of the matte side of the foil. The thin metal layer does not need to be removed after etching and acts as an oxide replacement and supplies enough adhesion to form a multilayer structure. Also, the metal layer is more uniform and reflective than a conductive foil alone and is easily inspected using well known automatic optical inspection (AOI) equipment.

The following non-limiting examples serve to illustrate the invention.

EXAMPLE 1

A copper foil is treated on the shiny with copper nodules and a Zn-Cr barrier layer is applied. The matte side is also treated with nodules but is subsequently

treated with nickel. The foil is laminated to an epoxy impregnated fiberglass (with the shiny side against the material) to form a substrate. A liquid photoresist is applied to the substrate to a thickness of 12 microns and exposed with UV light through a mask to from an image. The photoresist is developed using potassium carbonate, exposing the nickel surface. The nickel is removed using a cupric chloride etch, exposing the copper underneath. The copper is etched using an ammonia based system to define the traces. The photoresist removed using a sodium hydroxide solution. Holes are punched in the perimeter of the substrate based on the image pattern. These will be used for registration. The traces are inspected using an automatic optical inspection machine and repaired if necessary (and allowed). The completed substrate with etched traces (core) is laminated between epoxy fiberglass with other cores (if required) with copper foil on the outside. This printed circuit board "blank" is drilled, external circuitry defined, and completed by putting on soldermask and solder. The finished board is tested and then assembled.

EXAMPLE 2

Example 1 is repeated except the matte side of the laminate is against the substrate and is treated with Zn-Cr. The shiny side has nodules plated as in Example 1 but is treated with nickel.

EXAMPLE 3

Example 2 is repeated except the shiny surface is roughened by microetching prior to the nickel treatment.

EXAMPLE 4

Example 2 is repeated except the shiny side is roughened by pumice scrubbing prior to nickel treatment.

EXAMPLE 5

Example 1 is repeated except the photoresist is of a permanent nature and is not removed after etching.

EXAMPLE 6

Example 1 is repeated except etching is done in one step with cupric chloride.

EXAMPLE 7

Example 1 is repeated except the photoresist is exposed using a direct laser imaging system.

EXAMPLE 8

Example 1 is repeated except tin is plated in place of nickel and etching is done using nitric acid.

EXAMPLE 9

Copper foils are produced by electrodepositing copper from solution onto a rotating metal drum according to Example I of U.S. patent 3,293,109. Copper is dissolved in sulfuric acid and then electrodeposited in a solution of 70-105

g/L of copper as copper sulfate, 80-160 g/L of free sulfuric acid, at 40 –60 degrees C. The solution is brought into contact with a rotating metal dram, usually of titanium, which acts as a cathode and receives the copper as it is deposited from solution. The anode is constructed from a lead alloy. A cell voltage of about 5 to 10 volts is applied between the anode and the cathode to cause the copper to be deposited, while oxygen is evolved at the anode. Copper builds up a continuous film of copper on the drum at a thickness of from about 18 to 70 μm, which is removed, slit to the required width and finally wound in rolls. The side of the foil next to the drum is smooth (the "shiny side") while the other side has a relatively rough surface (the "matte side").

Samples of the copper foil are treated on either of the shiny or matte sides to produce surface nodules according to U.S. patent 5,679,230. Other samples of the copper foil are microetched with cupric chloride on either of the shiny or matte sides. Samples of the copper are measured for surface roughness and peel strength. Surface roughness is measured according to IPC-TM-650 Section 2.2.17 and peel strength is measured according to IPC-TM-650 Section 2.4.8 Revision C. The following results are noted:

Copper Foil Side	Treatment	Surface Roughness (Ra in microns)	Peel Strength* (kg/ linear cm)
Shiny	None	0.25	<0.18
Shiny	Micro-etch	1.20	0.39
Shiny	Nodules	3.56	1.52
Matte	None	5.08	0.63
Matte	Micro-etch	5.72	0.93
Matte	Nodules	7.60	1.91

* Peel strength was determined by laminating the copper to an epoxy prepreg. This simulates the peel strength inside the finished circuit board.

While the present invention has been particularly shown and described with reference to preferred embodiments, it will be readily appreciated by those of ordinary skill in the art that various changes and modifications may be made without departing from the spirit and scope of the invention. It is intended that the claims be interpreted to cover the disclosed embodiment, those alternatives which have been discussed above and all equivalents thereto.

What is claimed is:

1. A process for producing a printed circuit layer comprising conducting steps (a) and (b) in either order:

a) depositing a first surface of an electrically conductive layer onto a substrate, which electrically conductive layer has a roughened second surface opposite to the first surface;

b) depositing a thin metal layer onto the roughened second surface of the electrically conductive layer, which metal layer comprises a material having a different etch resistance property than that of the electrically conductive layer; and then

c) depositing a photoresist onto the metal layer;

d) imagewise exposing and developing the photoresist, thereby revealing underlying portions of the metal layer;

e) removing the revealed underlying portions of the metal layer, thereby revealing underlying portions of the conductive layer; and

f) removing the revealed underlying portions of the conductive layer, to thereby produce a printed circuit layer.

2. The process of claim 1 wherein step a) is conducted and then step b) is conducted.

3. The process of claim 1 wherein step b) is conducted and then step a) is conducted.

4. The process of claim 1 wherein step a) is conducted by first roughening the second surface of the electrically conductive layer, then treating with a second metal, and then depositing the first surface of the electrically conductive layer onto the substrate.

5. The process of claim 1 wherein step a) is conducted by first roughening the second surface of the electrically conductive layer and then depositing the first surface of the electrically conductive layer onto the substrate.

6. The process of claim 1 wherein step a) is conducted by first depositing the first surface of the electrically conductive layer onto the substrate and then roughening the second surface of the electrically conductive layer.

7. The process of claim 1 wherein the roughened second surface of the electrically conductive layer has an average roughness (Ra) value that ranges from about 1 to about 10 microns.

8. The process of claim 1 wherein the roughened second surface of the electrically conductive layer comprises micro-nodules of a metal or metal alloy on or in the roughened second surface.

9. The process of claim 1 wherein the roughened second surface of the electrically conductive layer is micro-etched.

10. A process for producing a composite which comprises repeating steps a) through f) of claim 1 at least once to thereby produce a plurality of printed circuit layers and then subsequently attaching the printed circuit layers to each other via at least one intermediate stratum thus forming a printed circuit board.

11. The process of claim 1 further comprising the step of removing any remaining photoresist after step (e).

12. The process of claim 1 further comprising the step of removing any remaining photoresist after step (f).

13. The process of claim 1 wherein the electrically conductive layer comprises an electrically conductive foil.

14. The process of claim 1 wherein the metal layer comprises a metal foil.

15. The process of claim 1 wherein the conductive layer comprises a material selected from the group consisting of copper , brass, stainless steel, aluminum, nickel and alloys and combinations thereof.

16. The process of claim 1 wherein the conductive layer is a copper foil.

17. The process of claim 1 wherein the conductive layer is laminated onto the substrate.

18. The process of claim 1 wherein the conductive layer is deposited onto the substrate by electrolytic or electroless deposition.

19. The process of claim 1 wherein the conductive layer is deposited onto the substrate by coating, sputtering, or evaporation.

20. The process of claim 1 wherein the metal layer comprises a material selected from the group consisting of nickel, tin, palladium, platinum, chromium, molybdenum, titanium and alloys and combinations thereof

21. The process of claim 1 wherein the metal layer comprises nickel.

22. The process of claim 1 wherein the metal layer comprises tin.

23. The process of claim 1 wherein the metal layer is laminated onto the conductive layer.

24. The process of claim 1 wherein the metal layer is deposited onto the conductive layer by either electrolytic or electroless deposition techniques.

25. The process of claim 1 wherein the metal layer is deposited onto the conductive layer by coating, sputtering, or evaporation.

26. The process of claim 1 wherein the revealed portions of the metal layer are removed by acid etching.

27. The process of claim 1 wherein the revealed portions of the conductive layer are removed by alkaline etching.

28. The process of claim 1 wherein the revealed portions of the metal layer and the underlying portions of the conductive layer are simultaneously removed by acid etching.

29. The process of claim 1 wherein the substrate comprises a polymer film.

30. The process of claim 1 wherein the substrate comprises a polyimide, polyester, or liquid crystal polymer film.

31. The process of claim 1 wherein the substrate comprises a reinforced polymer.

32. The process of claim 1 wherein the substrate comprises a reinforced polymer which comprises an epoxy, polyimide, cyanate ester, BT-Epoxy or combinations thereof.

33. The process of claim 1 wherein the substrate comprises a reinforced polymer wherein the reinforcement comprises fiberglass or an organic paper .

34. A printed circuit layer produced by the process of conducting steps a) and b) in either order:

a) depositing a first surface of an electrically conductive layer onto a substrate, which electrically conductive layer has a roughened second surface opposite to the first surface;

b) depositing a thin metal layer onto the roughened second surface of the electrically conductive layer, which metal layer comprises a material having a different etch resistance property than that of the electrically conductive layer; and then

c) depositing a photoresist onto the metal layer;

d) imagewise exposing and developing the photoresist, thereby revealing underlying portions of the metal layer;

e) removing the revealed underlying portions of the metal layer, thereby revealing underlying portions of the conductive layer; and

f) removing the revealed underlying portions of the conductive layer.

35. The printed circuit layer of claim 34 wherein the electrically conductive layer comprises an electrically conductive foil

36. The printed circuit layer of claim 34 wherein the metal layer comprises a metal foil.

37. The printed circuit layer of claim 34 wherein the conductive layer comprises a material selected from the group consisting of copper , brass, stainless steel, aluminum, nickel and alloys and combinations thereof .

38. The printed circuit layer of claim 34 wherein the conductive layer comprises a copper foil.

38. The printed circuit layer of claim 34 wherein the metal layer comprises a material selected from the group consisting of nickel, tin, palladium, platinum, chromium, molybdenum, titanium and alloys and combinations thereof .

39. The printed circuit layer of claim 34 wherein the metal layer comprises nickel.

40. The printed circuit layer of claim 34 wherein the metal layer comprises tin.

41. The printed circuit layer of claim 34 wherein the substrate comprises a semiconductor.

42. The printed circuit layer of claim 34 wherein the substrate comprises gallium arsenide, silicon, compositions containing silicon and combinations thereof.

INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER
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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	EP 0 758 840 A (MITSUI MINING & SMELTING CO) 19 February 1997 (1997-02-19) page 3, line 45 -page 4, line 39 ---	1-5,7,8, 10, 12-17, 20,21, 24,28-39
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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

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Date of the actual completion of the international search	Date of mailing of the international search report
5 April 2002	12/04/2002

Name and mailing address of the ISA	Authorized officer
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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 01/32400

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
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Information on patent family members

International Application No
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(54) Title: USE OF METALLIC TREATMENT ON COPPER FOIL TO PRODUCE FINE LINES AND REPLACE OXIDE PROCESS IN PRINTED CIRCUIT BOARD PRODUCTION

(57) Abstract: The invention relates to the manufacture of printed circuit boards having enhanced etch uniformity and resolution. The process eliminates the need for a black oxide treatment to improve adhesion and improves the ability to optically inspect the printed circuit boards. The process is performed by conducting steps (a) and (b) in either order: a) depositing a first surface of an electrically conductive layer onto a substrate, which electrically conductive layer has a roughened second surface opposite to the first surface; b) depositing a thin metal layer onto the roughened second surface of the electrically conductive layer, which metal layer comprises a material having a different etch resistance property than that of the electrically conductive layer. Thereafter one deposits a photoresist onto the metal layer; imagewise exposes and develops the photoresist, thereby revealing underlying portions of the metal layer. The one removes the revealed underlying portions of the metal layer, thereby revealing underlying portions of the conductive layer and removes the revealed underlying portions of the conductive layer, to thereby produce a printed circuit layer.

USE OF METALLIC TREATMENT ON COPPER FOIL TO PRODUCE FINE LINES AND REPLACE OXIDE PROCESS IN PRINTED CIRCUIT BOARD PRODUCTION

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The present invention relates to the manufacture of printed circuit boards having enhanced etch uniformity and resolution. The process of this invention eliminates the need for a black oxide treatment to improve adhesion and improves the ability to optically inspect the printed circuit boards.

DESCRIPTION OF THE RELATED ART

Printed circuit boards have wide application in the field of electronics. They are useful for large scale applications, such as in missiles and industrial control equipment, as well as in small scale devices, such as telephones, radios and personal computers. In particular, when utilizing printed circuits it is important that a high degree of accuracy and resolution is attained for very small line and space widths (on the order of one hundred microns or less) to ensure good performance of the circuit.

The ability to produce accurate features having very small dimensions, on the order of one hundred microns or less, is extremely important in the production of small and large scale equipment. The precision of the etching process becomes more important as the circuit patterns become ever smaller. It is well known in the art to use known photolithographic techniques to produce printed circuit boards having small features with high accuracy. In general, an electrically conductive foil is deposited onto a substrate and a photoresist is

then deposited onto the foil. That photoresist is then imagewise exposed and developed, forming a pattern of small lines and spaces that are then etched into the conductive foil.

Conventionally a matte side of a foil is laminated onto the substrate, mainly because the matte side of the foil is rougher and has better adhesion to the substrate than the shiny side of the foil. However, it has been found that by laminating the foil with the shiny side down against the substrate that much more accurate etching could be achieved because the copper grains are elongated and oriented vertically near the matte side and less side or horizontal etching occurs. In addition, there is less of a need to over etch to remove the tooth structure and treatment from the substrate, which results in better etch uniformity.

When laminating the shiny side of the foil onto a substrate, it is necessary to roughen the surface to provide sufficient adhesion. One method to accomplish this is to plate nodules to the shiny side of a copper foil. An example of this type of copper product is commercially available from Oak-Mitsui Inc., of Hoosick Falls, N.Y. as MLS. Another method that has been used is to deposit roughening layers, such as nodules, on each side of the foil, forming "double treated" foils. With this process one gets superior resist adhesion, as well as the elimination of the oxide process. This has not been preferred in the industry because the exposed side of the foil may have the roughening layer damaged during handling.

When the matte side is against the laminate another known method of roughening the shiny layer is a process in which a copper foil is pre-roughened by chemical micro etching (using sodium persulfate or sulfuric acid/hydrogen peroxide which are available from MacDermid of Waterbury CT or Shipley

Ronel of Marborough MA) or pumice scrubbing (machines available from I.S of Italy and Isioki of Japan) . The surface is later chemically treated to deposit a layer of black copper oxide (also available from MacDermid and Shipley Ronel), allowing another insulating substrate to be laminated over the circuit. This sequence of chemical treatments is undesirable because it is cumbersome and introduces waste disposal problems with the chemicals used. Therefore, there is a need in the art for a process that does not have the problems of double treating a conductive foil and which does not need a black oxide treatment during the processing of multi-layer circuit boards, that will etch circuit lines and spaces with high resolution and accuracy.

Efforts are continuously being made in the art to improve techniques by which circuit boards are manufactured and thus the accuracy of these features. For example, see U.S. patent 5,240,807 which teaches a photoresist article having a portable, conformable, built-on etch mask useful for enhancing image contrast and reproducing parts having very small dimensions. Portions of a conductive foil underlying the photoresist are selectively etched to form a pattern of circuit lines. Another approach is disclosed in U.S. patent 6,042,711 which provides a metal foil with improved peel strength having a metal layer of a dusty dendritic deposit and a metal flash layer. Additionally, International Publication WO 00/03568 discloses a method of forming circuit lines on a substrate by applying a roughened conductive metal layer using a copper foil carrier.

In yet another approach, U.S. patent 5,679,230 provides a copper foil for use in the manufacture of printed circuit boards. This copper foil can be used to make multilayer circuit boards without requiring the conventional black oxide treatment to improve adhesion.

The present invention provides an approach to solving the problems of the prior art wherein a thin metal layer is deposited onto a conductive layer on a substrate. This metal layer acts as an etch mask during etching of the conductive layer, and improves etch accuracy and resolution. After etching, this thin metal layer remains on the conductive layer obviating the need for an oxide layer.

The metal layers employed in this process are also highly uniform and reflective, making the printed circuits formed thereby more compatible with automatic optical inspection equipment than printed circuits of the prior art. Further, the metal layers used herein have high mechanical strength, and are highly resistant to mechanical damage, such as surface scratches and scuff marks.

SUMMARY OF THE INVENTION

The invention provides a process for producing a printed circuit layer comprising conducting steps (a) and (b) in either order:

a) depositing a first surface of an electrically conductive layer onto a substrate, which electrically conductive layer has a roughened second surface opposite to the first surface;

b) depositing a thin metal layer onto the roughened second surface of the electrically conductive layer, which metal layer comprises a material having a different etch resistance property than that of the electrically conductive layer; and then

c) depositing a photoresist onto the metal layer;

d) imagewise exposing and developing the photoresist, thereby revealing underlying portions of the metal layer;

e) removing the revealed underlying portions of the metal layer, thereby revealing underlying portions of the conductive layer; and

f) removing the revealed underlying portions of the conductive layer, to thereby produce a printed circuit layer.

The invention also provides a printed circuit layer produced by the process of conducting steps a) and b) in either order:

a) depositing a first surface of an electrically conductive layer onto a substrate, which electrically conductive layer has a roughened second surface opposite to the first surface;

b) depositing a thin metal layer onto the roughened second surface of the electrically conductive layer, which metal layer comprises a material having a different etch resistance property than that of the electrically conductive layer; and then

c) depositing a photoresist onto the metal layer;

d) imagewise exposing and developing the photoresist, thereby revealing underlying portions of the metal layer;

e) removing the revealed underlying portions of the metal layer, thereby revealing underlying portions of the conductive layer; and

f) removing the revealed underlying portions of the conductive layer.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The invention broadly provides a process for producing a printed circuit layer and printed circuit board.

The first step in conducting the process of the present invention is to deposit a layer of an electrically conductive material onto a suitable substrate. Typical substrates are those suitable to be processed into a printed circuit or other microelectronic device. Suitable substrates for the present invention non-exclusively include polymers reinforced with materials such as fiberglass, aramid (Kevlar), aramid paper (Thermount), polybenzoxolate paper or

combinations thereof. Of these epoxy with fiberglass reinforcement is the most preferred substrate. Also suitable are semiconductor materials such as gallium arsenide (GaAs), silicon and compositions containing silicon such as crystalline silicon, polysilicon, amorphous silicon, epitaxial silicon, and silicon dioxide (SiO_2) and mixtures thereof. The preferred thickness of the substrate is of from about 10 to about 200 microns, more preferably from about 10 to about 50 microns.

The conductive layer preferably comprises a material such as copper, zinc, brass, chrome, , nickel, aluminum, stainless steel, iron, gold, silver, titanium and combinations and alloys thereof. Most preferably, the conductive layer is a copper foil.

Copper foils are preferably produced by electrodepositing copper from solution onto a rotating metal drum. The side of the foil next to the drum is typically the smooth or shiny side, while the other side has a relatively rough surface, also known as the matte side. This drum is usually made of stainless steel or titanium which acts as a cathode and receives the copper as it is deposited from solution. An anode is generally constructed from a lead alloy. A cell voltage of about 5 to 10 volts is applied between the anode and the cathode to cause the copper to be deposited, while oxygen is evolved at the anode. This copper foil is then removed from the drum, cut to the required size, and laminated onto the substrate. Lamination is preferably conducted in a press at a minimum of about 175°C, for about 30 minutes. Preferably, the press is under a vacuum of at least 28 inches of mercury, and maintained at a pressure of about 150 psi.

Preferably but not necessarily prior to lamination, the conductive foil is preferably, but not necessarily, electrolytically treated on the shiny side to form

a roughening copper deposit, and electrolytically treated on the matte side to deposit micro nodules of a metal or alloy. These nodules are preferably copper or a copper alloy, and do not add roughness to the surface, but do increase adhesion to a substrate. The surface microstructure of the foil is measured by a profilometer, such as a Perthometer model M4P or S5P which is commercially available from Mahr Feinpruef Corporation of Cincinnati, Ohio. Topography measurements of the surface grain structure of peaks and valleys are made according to industry standard IPC-TM-650 Section 2.2.17 of the Institute for Interconnecting and Packaging Circuits of 2115 Sanders Road, Northbrook, Illinois 60062. In the measurement procedure, a measurement length Im over the sample surface is selected. Rz defined as the average maximum peak to valley height of five consecutive sampling lengths within the measurement length Im (where Io is Im/5). Rt is the maximum roughness depth and is the greatest perpendicular distance between the highest peak and the lowest valley within the measurement length Im. Rp is the maximum leveling depth and is the height of the highest peak within the measuring length Im. Ra, or average roughness, is defined as the arithmetic average value of all absolute distances of the roughness profile from the center line within the measuring length Im.

The parameters of importance for this invention are Rz and Ra. The surface treatments carried out produce a surface structure having peaks and valleys, which produce roughness parameters wherein Ra ranges from about 1 to about 10 microns and Rz ranges from about 2 to about 10 microns.

The surface treatments carried out produce a surface structure having peaks and valleys, on the shiny side, which produce roughness parameters wherein Ra ranges from about 1 to about 4 microns, preferably from about 2 to about 4 microns, and most preferably from about 3 to about 4 microns. The Rz value

ranges from about 2 to about 4.5 microns, preferably from about 2.5 to about 4.5 microns, and more preferably from about 3 to about 4.5 microns.

The surface treatments carried out produce a surface structure having peaks and valleys, on the matte side, which produce roughness parameters wherein Ra ranges from about 4 to about 10 microns, preferably from about 4.5 to about 8 microns, and most preferably from about 5 to about 7.5 microns. The Rz value ranges from about 4 to about 10 microns, preferably from about 4 to about 9 microns, and more preferably from about 4 to about 7.5 microns.

Preferably, the shiny side has a copper deposit about 2 to 4.5 μm thick to produce an average roughness (Rz) of 2 μm or greater. The matte side preferably will have a roughness Rz as made of about 4-7.5 μm. The micro nodules of metal or alloy will have a size of about 0.5 μm. Other metals may be deposited as micro nodules if desired, for example, zinc, indium, tin, cobalt, brass, bronze and the like. This process is more thoroughly described in U.S. patent 5,679,230, which is incorporated herein by reference. The shiny surface has a peel strength ranging from about .7 kg/linear cm to about 1.6 kg/linear, preferably from about .9 kg/linear cm to about 1.6 kg/linear. The matte surface has a peel strength ranging from about .9 kg/linear cm to about 2 kg/linear, preferably from about 1.1 kg/linear cm to about 2 kg/linear. Peel strength is measured according to industry standard IPC-TM-650 Section 2.4.8 Revision C.

The conductive layer preferably has a thickness of from about 0.5 to about 200 microns, more preferably from about 9 to about 70 microns. The conductive layer may also be applied using any other well known method of metal deposition such as electroless deposition, coating, sputtering, evaporation or by lamination onto the substrate.

Also preferably but not necessarily prior to lamination, the foil is preferably, but not necessarily, electrolytically treated on either side with, a thin metal layer. This metal layer is preferably electrolytically deposited onto the conductive layer. The metal layer may also be deposited onto the conductive layer (after laminating to the substrate) by coating, sputtering, evaporation or by lamination onto the conductive layer. Preferably the metal layer is a thin film and comprises a material selected such as nickel, tin, palladium platinum, chromium, titanium, molybdenum or alloys thereof. Most preferably the metal layer comprises nickel or tin. The metal layer preferably has a thickness of from about .01 to about 10 microns, more preferably from about .2 to about 3 microns. This metal layer will serve as an etch mask to define a pattern of circuit lines and spaces to be etched into the conductive layer.

Once the metal layer is deposited onto the conductive layer, the next step is to selectively etch away portions of the metal layer, forming an etched pattern in the metal layer. This etched pattern is formed by well known photolithographic techniques using a photoresist composition.. First, a photoresist deposited directly onto the thin metal layer. The photoresist composition may be positive working or negative working and is generally commercially available. The resist can be very thin (5 to 20 microns) since it's main function is to only define the thin metal layer and does not need to withstand severe etch conditions. This allows much greater resolution. Suitable positive working photoresists are well known in the art and may comprise an o-quinone diazide radiation sensitizer. The o-quinone diazide sensitizers include the o-quinone-4-or-5-sulfonyl-diazides disclosed in U. S. Patents Nos. 2,797,213; 3,106,465; 3,148,983; 3,130,047; 3,201,329; 3,785,825; and 3,802,885. When o-quinone diazides are used, preferred binding resins include a water insoluble, aqueous alkaline soluble or swellable

binding resin, which is preferably a novolak. Suitable positive photodielectric resins may be obtained commercially, for example, under the trade name of AZ-P4620 from Clariant Corporation of Somerville, New Jersey as well as Shipley I-line photoresist. Negative photoresists are also widely commercially available.

The photoresist is then imagewise exposed to actinic radiation such as light in the visible, ultraviolet or infrared regions of the spectrum through a mask, or scanned by an electron beam, ion or neutron beam or X-ray radiation. Actinic radiation may be in the form of incoherent light or coherent light, for example, light from a laser. The photoresist is then imagewise developed using a suitable solvent, such as an aqueous alkaline solution, thereby revealing underlying portions of the metal layer.

Subsequently, the revealed underlying portions of the metal layer are removed through well known etching techniques while not removing the portions underlying the remaining photoresist. Suitable etchants non-exclusively include acidic solutions, such as cupric chloride (preferable for etching of nickel) or nitric acid (preferable for etching of tin). Also preferred are ferric chloride or sulfuric peroxide (hydrogen peroxide with sulfuric acid). During this step, the portions of the conductive layer underlying the etched off portions of the metal layer are revealed. This patterned metal layer defines an excellent quality etch mask for etching the conductive layer with high accuracy and precision.

Next, the revealed underlying portions of the conductive layer are removed by etching while not removing the portions of the conductive layer underlying the non-removed portions of the metal layer. Suitable etchants for removing the conductive layer non-exclusively include alkaline solutions, such as

ammonium chloride/ammonium hydroxide. This circuit board may then be rinsed and dried. The result is a printed circuit board having excellent resolution and uniformity, and having excellent performance.

In another preferred embodiment wherein the metal layer comprises nickel, a one pass etching process may be conducted. In this embodiment, after the photoresist has been imaged and developed, each of the revealed portions of the metal layer and the underlying electrically conductive layer may be etched in a cupric chloride etcher. For etching of other metal layers, including Tin, the appropriate etchant is unable to properly etch the underlying conductive foil and a second etching step is still required. This single etching step is preferred for etching lines or spaces of greater than about 3 mils. When a single etching step is used, it may also be necessary to increase the dwell time in the etcher by possibly 10 to 25% depending on the etch system. .Higher spray pressures and temperature may accomplish the same results.
After the circuit lines and spaces are etched through the metal layer and the conductive layer, the remaining photoresist can optionally be removed from the metal layer surface either by stripping with a suitable solvent or by ashing by well known ashing techniques. The photoresist may also be removed after etching the metal layer, but prior to etching the conductive foil.

In a preferred ashing process, plasma is generated in a microwave plasma generator located upstream of a stripping chamber and stripping gases pass through this generator so that reactive species produced from the gases in the plasma enter the stripping chamber. Plasma ions are removed such as by filtering from plasma radicals. The term "radical", as used herein is intended to define uncharged particles such as atoms or molecular fragments which are generated by the upstream plasma generator. The plasma generator may comprise any plasma generator known in the art. Plasma generators which are

capable of providing a source of radicals, substantially without ions or electrons, are described, for example, in U.S. patent 5,174,856 and U.S. patent 5,200,031, the disclosures of which are hereby incorporated by reference. While any type of conventionally generated plasma may, in general, be used in the practice of the invention, preferably the plasma used is generated by a microwave plasma generator such as, for example, a Model AURA plasma generator commercially available from the GaSonics of San Jose, Calif. Another upstream plasma generator which is capable of supplying a source of radicals in the substantial absence of electrons and/or ions is commercially available from Applied Materials, Inc. as an Advanced Strip Passivation (ASP) Chamber. Plasma ashers are also commercially available from Mattson Technology of Fremont, California. Ashing may also be performed in an anisotropic method through the use of in situ ashing in an etch chamber such as a TEL DRM 85, available from Tokyo Electron Ltd.

At this point, another insulating substrate may be laminated over the circuit without an additional roughening step and without black oxide treatment of the matte side of the foil. The thin metal layer does not need to be removed after etching and acts as an oxide replacement and supplies enough adhesion to form a multilayer structure. Also, the metal layer is more uniform and reflective than a conductive foil alone and is easily inspected using well known automatic optical inspection (AOI) equipment.

The following non-limiting examples serve to illustrate the invention.

EXAMPLE 1

A copper foil is treated on the shiny with copper nodules and a Zn-Cr barrier layer is applied. The matte side is also treated with nodules but is subsequently

treated with nickel. The foil is laminated to an epoxy impregnated fiberglass (with the shiny side against the material) to form a substrate. A liquid photoresist is applied to the substrate to a thickness of 12 microns and exposed with UV light through a mask to from an image. The photoresist is developed using potassium carbonate, exposing the nickel surface. The nickel is removed using a cupric chloride etch, exposing the copper underneath. The copper is etched using an ammonia based system to define the traces. The photoresist removed using a sodium hydroxide solution. Holes are punched in the perimeter of the substrate based on the image pattern. These will be used for registration. The traces are inspected using an automatic optical inspection machine and repaired if necessary (and allowed). The completed substrate with etched traces (core) is laminated between epoxy fiberglass with other cores (if required) with copper foil on the outside. This printed circuit board "blank" is drilled, external circuitry defined, and completed by putting on soldermask and solder. The finished board is tested and then assembled.

EXAMPLE 2

Example 1 is repeated except the matte side of the laminate is against the substrate and is treated with Zn-Cr. The shiny side has nodules plated as in Example 1 but is treated with nickel.

EXAMPLE 3

Example 2 is repeated except the shiny surface is roughened by microetching prior to the nickel treatment.

EXAMPLE 4

Example 2 is repeated except the shiny side is roughened by pumice scrubbing prior to nickel treatment.

EXAMPLE 5

Example 1 is repeated except the photoresist is of a permanent nature and is not removed after etching.

EXAMPLE 6

Example 1 is repeated except etching is done in one step with cupric chloride.

EXAMPLE 7

Example 1 is repeated except the photoresist is exposed using a direct laser imaging system.

EXAMPLE 8

Example 1 is repeated except tin is plated in place of nickel and etching is done using nitric acid.

EXAMPLE 9

Copper foils are produced by electrodepositing copper from solution onto a rotating metal drum according to Example I of U.S. patent 3,293,109. Copper is dissolved in sulfuric acid and then electrodeposited in a solution of 70-105

g/L of copper as copper sulfate, 80-160 g/L of free sulfuric acid, at 40 –60 degrees C. The solution is brought into contact with a rotating metal dram, usually of titanium, which acts as a cathode and receives the copper as it is deposited from solution. The anode is constructed from a lead alloy. A cell voltage of about 5 to 10 volts is applied between the anode and the cathode to cause the copper to be deposited, while oxygen is evolved at the anode. Copper builds up a continuous film of copper on the drum at a thickness of from about 18 to 70 μm, which is removed, slit to the required width and finally wound in rolls. The side of the foil next to the drum is smooth (the "shiny side") while the other side has a relatively rough surface (the "matte side").

Samples of the copper foil are treated on either of the shiny or matte sides to produce surface nodules according to U.S. patent 5,679,230. Other samples of the copper foil are microetched with cupric chloride on either of the shiny or matte sides. Samples of the copper are measured for surface roughness and peel strength. Surface roughness is measured according to IPC-TM-650 Section 2.2.17 and peel strength is measured according to IPC-TM-650 Section 2.4.8 Revision C. The following results are noted:

Copper Foil Side	Treatment	Surface Roughness (Ra in microns)	Peel Strength* (kg/ linear cm)
Shiny	None	0.25	<0.18
Shiny	Micro-etch	1.20	0.39
Shiny	Nodules	3.56	1.52
Matte	None	5.08	0.63
Matte	Micro-etch	5.72	0.93
Matte	Nodules	7.60	1.91

* Peel strength was determined by laminating the copper to an epoxy prepreg. This simulates the peel strength inside the finished circuit board.

While the present invention has been particularly shown and described with reference to preferred embodiments, it will be readily appreciated by those of ordinary skill in the art that various changes and modifications may be made without departing from the spirit and scope of the invention. It is intended that the claims be interpreted to cover the disclosed embodiment, those alternatives which have been discussed above and all equivalents thereto.

What is claimed is:

1. A process for producing a printed circuit layer comprising conducting steps (a) and (b) in either order:

a) depositing a first surface of an electrically conductive layer onto a substrate, which electrically conductive layer has a roughened second surface opposite to the first surface;

b) depositing a thin metal layer onto the roughened second surface of the electrically conductive layer, which metal layer comprises a material having a different etch resistance property than that of the electrically conductive layer; and then

c) depositing a photoresist onto the metal layer;

d) imagewise exposing and developing the photoresist, thereby revealing underlying portions of the metal layer;

e) removing the revealed underlying portions of the metal layer, thereby revealing underlying portions of the conductive layer; and

f) removing the revealed underlying portions of the conductive layer, to thereby produce a printed circuit layer.

2. The process of claim 1 wherein step a) is conducted and then step b) is conducted.

3. The process of claim 1 wherein step b) is conducted and then step a) is conducted.

4. The process of claim 1 wherein step a) is conducted by first roughening the second surface of the electrically conductive layer, then treating with a second metal, and then depositing the first surface of the electrically conductive layer onto the substrate.

5. The process of claim 1 wherein step a) is conducted by first roughening the second surface of the electrically conductive layer and then depositing the first surface of the electrically conductive layer onto the substrate.

6. The process of claim 1 wherein step a) is conducted by first depositing the first surface of the electrically conductive layer onto the substrate and then roughening the second surface of the electrically conductive layer.

7. The process of claim 1 wherein the roughened second surface of the electrically conductive layer has an average roughness (Ra) value that ranges from about 1 to about 10 microns.

8. The process of claim 1 wherein the roughened second surface of the electrically conductive layer comprises micro-nodules of a metal or metal alloy on or in the roughened second surface.

9. The process of claim 1 wherein the roughened second surface of the electrically conductive layer is micro-etched.

10. A process for producing a composite which comprises repeating steps a) through f) of claim 1 at least once to thereby produce a plurality of printed circuit layers and then subsequently attaching the printed circuit layers to each other via at least one intermediate stratum thus forming a printed circuit board.

11. The process of claim 1 further comprising the step of removing any remaining photoresist after step (e).

12. The process of claim 1 further comprising the step of removing any remaining photoresist after step (f).

13. The process of claim 1 wherein the electrically conductive layer comprises an electrically conductive foil.

14. The process of claim 1 wherein the metal layer comprises a metal foil.

15. The process of claim 1 wherein the conductive layer comprises a material selected from the group consisting of copper , brass, stainless steel, aluminum, nickel and alloys and combinations thereof.

16. The process of claim 1 wherein the conductive layer is a copper foil.

17. The process of claim 1 wherein the conductive layer is laminated onto the substrate.

18. The process of claim 1 wherein the conductive layer is deposited onto the substrate by electrolytic or electroless deposition.

19. The process of claim 1 wherein the conductive layer is deposited onto the substrate by coating, sputtering, or evaporation.

20. The process of claim 1 wherein the metal layer comprises a material selected from the group consisting of nickel, tin, palladium, platinum, chromium, molybdenum, titanium and alloys and combinations thereof

21. The process of claim 1 wherein the metal layer comprises nickel.

22. The process of claim 1 wherein the metal layer comprises tin.

23. The process of claim 1 wherein the metal layer is laminated onto the conductive layer.

24. The process of claim 1 wherein the metal layer is deposited onto the conductive layer by either electrolytic or electroless deposition techniques.

25. The process of claim 1 wherein the metal layer is deposited onto the conductive layer by coating, sputtering, or evaporation.

26. The process of claim 1 wherein the revealed portions of the metal layer are removed by acid etching.

27. The process of claim 1 wherein the revealed portions of the conductive layer are removed by alkaline etching.

28. The process of claim 1 wherein the revealed portions of the metal layer and the underlying portions of the conductive layer are simultaneously removed by acid etching.

29. The process of claim 1 wherein the substrate comprises a polymer film.

30. The process of claim 1 wherein the substrate comprises a polyimide, polyester, or liquid crystal polymer film.

31. The process of claim 1 wherein the substrate comprises a reinforced polymer.

32. The process of claim 1 wherein the substrate comprises a reinforced polymer which comprises an epoxy, polyimide, cyanate ester, BT-Epoxy or combinations thereof.

33. The process of claim 1 wherein the substrate comprises a reinforced polymer wherein the reinforcement comprises fiberglass or an organic paper .

34. A printed circuit layer produced by the process of conducting steps a) and b) in either order:

a) depositing a first surface of an electrically conductive layer onto a substrate, which electrically conductive layer has a roughened second surface opposite to the first surface;

b) depositing a thin metal layer onto the roughened second surface of the electrically conductive layer, which metal layer comprises a material having a different etch resistance property than that of the electrically conductive layer; and then

c) depositing a photoresist onto the metal layer;

d) imagewise exposing and developing the photoresist, thereby revealing underlying portions of the metal layer;

e) removing the revealed underlying portions of the metal layer, thereby revealing underlying portions of the conductive layer; and

f) removing the revealed underlying portions of the conductive layer.

35. The printed circuit layer of claim 34 wherein the electrically conductive layer comprises an electrically conductive foil

36. The printed circuit layer of claim 34 wherein the metal layer comprises a metal foil.

37. The printed circuit layer of claim 34 wherein the conductive layer comprises a material selected from the group consisting of copper , brass, stainless steel, aluminum, nickel and alloys and combinations thereof .

38. The printed circuit layer of claim 34 wherein the conductive layer comprises a copper foil.

39. The printed circuit layer of claim 34 wherein the metal layer comprises a material selected from the group consisting of nickel, tin, palladium, platinum, chromium, molybdenum, titanium and alloys and combinations thereof .

40. The printed circuit layer of claim 34 wherein the metal layer comprises nickel.

41. The printed circuit layer of claim 34 wherein the metal layer comprises tin.

42. The printed circuit layer of claim 34 wherein the substrate comprises a semiconductor.

43. The printed circuit layer of claim 34 wherein the substrate comprises gallium arsenide, silicon, compositions containing silicon and combinations thereof.

INTERNATIONAL SEARCH REPORT

International Application No
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A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H05K3/06 H05K3/24 H05K3/38

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H05K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
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INTERNATIONAL SEARCH REPORT

International Application No
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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